IN THE CLAIMS:

1. A method for fabricating a floating gate transistor, the method comprising:

fabricating first and second laterally spaced trenches in a substrate, such that a vertically extending substrate island is formed;

implanting a source region in the substrate under the first and second trenches;

implanting a drain region in a top region of the substrate island;

fabricating a first dielectric layer adjacent to the substrate island in the second trench;

fabricating a floating gate adjacent to the first dielectric layer such that the first dielectric layer is between the floating gate and the substrate island;

fabricating a second dielectric layer adjacent to the floating gate;

fabricating a control gate adjacent to the second dielectric layer such that the second dielectric layer is between the control gate and the floating gate; and

filling the first trench with a dielectric material.

2. The method of claim 1 further comprising:

fabricating a word line coupled to the control gate and having a major axis extending in horizontal direction generally perpendicular to a major axis of the control gate.

3. The method of claim 1 wherein fabricating the floating gate comprises:

fabricating a layer of polysiliscon in the first trench such that vertical sides and a bottom of the trench is covered; and

etching the layer of polysilicon to form two floating gates.

4. A method for fabricating a plurality of floating gate transistors, the method comprising:

fabricating first, second, and third laterally spaced trenches in a substrate, such that two vertically extending substrate islands are formed;

implanting a source region in the substrate under the first, second, and third trenches;

implanting a drain region in a top region of the substrate islands;

fabricating a lower dielectric layer adjacent to each substrate island in the second trench;

fabricating a floating gate adjacent to each lower dielectric layer in the second trench such that one of the lower dielectric layers is between each floating gate and each substrate island;

fabricating an upper dielectric layer adjacent to each floating gate;

fabricating a control gate within the second trench and adjacent to the upper dielectric layers such that the upper dielectric layers are between the control gate and the floating gates; and

filling the first and second trenches with a dielectric material.

5. The method of claim 4 wherein the upper dielectric layer is an oxide-nitride-oxide layer.

6. The method of claim 4 wherein the control gate is a polysilicon material.